Amendments To The Claims:

Please amend the claims as shown.

1 – 22 (canceled)

23. (new) A circuit for clock synchronization between a first and a second network unit, comprising:

a clock recovery unit having at least one reference clock signal provided in the first network unit;

a bus provision unit with an encoding unit arranged in the first network unit where the encoding unit is used for creating a channel signal from the reference clock signal; and

a bus signal created from a plurality of channel signals and forwarded to a decoder unit in the second network unit.

24. (new) The circuit as claimed in claim 23, wherein the encoding unit is configured such that a sequence of individual pulses with a defined distance is created from the reference clock signal present on the input side.

25. (new) The circuit as claimed in claim 24, wherein the encoding unit is configured such that the defined distances of the pulses are different for each channel signal.

26. (new) The circuit as claimed in claim 25, wherein the encoding unit is configured such that the number of pulses created in each channel signal corresponds to the maximum possible number(s) of the encoding units.

27. (new) The circuit as claimed in claim 26, wherein the encoding unit is configured so:

the width of the created pulses are different,

the width of the pulses created are embodied in ascending order, and

no distinction is made with regard to pulse width formation below the encoding units.

28. (new) The circuit as claimed in claim 27, wherein the bus provision unit is configured so the channel signals are grouped together via a summation unit and signal amplification unit into a bus signal.

29. (new) The circuit as claimed in claim 23, wherein the decoding unit has a pulse width filter and a pulse distance filter.

30. (new) The circuit as claimed in claim 29, wherein the decoding unit is configured so that decoding is performed by a mask function, where the received bus signal is not sampled and the selection occurs by masking out the non required pulses.

31. (new) The circuit as claimed in claim 30, wherein the created pulses having different pulse width and pulse distance are coordinated for simultaneous collision free real-time transmission of the clock signals.

32. (new) The circuit as claimed in claim 31, wherein the selection of an individual channel signal from the bus signal is performed independently by the second network unit.

33. (new) A method for clock synchronization between a first and second network unit, comprising:

providing a reference clock signal in the first network unit by a clock recovery unit;

forming a channel signal from a reference clock signal where in the first network unit a bus signal being formed from at least one channel signal and forwarded to the second network unit;

creating pulses having different pulse width and pulse distance; and

coordinating the pulse distance and pulse width encoding for simultaneous collision free real-time transmission of the clock signals.

34. (new) The method as claimed in 33, wherein a sequence of individual pulses with a defined distance is created from the reference clock signal present on the input side.

35. (new) The method as claimed in 34, wherein the defined distances of the pulses are characterized differently in each channel signal and the number of pulses generated in each channel signal corresponds to a maximum possible number of the encoding units.

36. (new) The method as claimed in claim 35, wherein the created pulses are created in ascending order relative to their pulse width.

37. (new) The method as claimed in claim 36, wherein pulse width formation is not considered below the encoding units.

38. (new) The method as claimed in claim 37, wherein the channel signals are grouped into a bus signal.

39. (new) The method as claimed in claim 38, wherein the individual channel signals are selected from the bus signal independently by the second network unit.

40. (new) The method as claimed in 39, wherein decoding is performed in the second network unit by a mask function, where the received bus signal is not sampled and the selection is made by masking out the un-required pulses.

41. (new) A circuit for clock synchronization between a first and a second network unit, comprising:

a clock recovery unit having at least one reference clock signal provided in the first network unit;

a bus provision unit with an encoding unit arranged in the first network unit where the encoding unit is used for creating a channel signal from the reference clock signal; where created pulses having different pulse width and pulse distance are coordinated for simultaneous collision free real-time transmission of the clock signals; and

a bus signal created a plurality of channel signals and forwarded to a decoder unit in the second network unit where the selection of an individual channel signal from the bus signal is performed independently by the second network unit.